WHAT IS CLAIMED IS:

1. A method of modeling a combinatorial gate comprising:
providing a data signal input at the combinatorial gate;
providing a clock signal input at the combinatorial gate; and,
propagating the clock signal as an output signal when the output of the combinatorial gate corresponds to the clock signal; and,
propagating the data signal as an output when the output of the combinatorial gate corresponds to the data signal, the propagating the data signal modeling a near domino function.

2. The method of claim 1 wherein:
the near domino function is propagated based upon performing a reverse traversal function on a circuit design containing the combinatorial gate.

3. The method of claim 1 wherein:
the near domino function includes causing a later arriving edge of the data signal to cause the output signal to respond.

4. The method of claim 1 wherein:
the data signal includes a single edge per clock period; and,
when providing the near domino function, the single edge is propagated through the combinatorial gate.

5. The method of claim 1 wherein:
the clock signal includes two edges per clock period; and,
when propagating the clock signal, the two edges are propagated through the combinatorial gate.

6. A method of determining how to model a combinatorial gate where the combinatorial gate receives a data signal and a clock signal comprising:

performing a reverse traversal function on a circuit containing the combinatorial gate,

modeling an output of the combinatorial gate as the clock signal when an input to a next element of the circuit is a clock; and,

modeling the output of the combinatorial gate as a data signal when an input to a next element of the circuit is a data signal.

7. The method of claim 6 wherein:

the modeling the output of the combinatorial gate as a data signal includes a near domino function.

8. The method of claim 7 wherein:

the near domino function includes causing a later arriving edge of the data signal to cause the output signal to respond.

9. The method of claim 7 wherein:

the data signal includes a single edge per clock period; and,

when providing the near domino function, the single edge is propagated through the combinatorial gate.

10. The method of claim 7 wherein:

the clock signal includes two edges per clock period; and,

when propagating the clock signal, the two edges are propagated through the combinatorial gate.

11. A method of modeling a combinatorial gate within a static timing analysis comprising:

receiving a data signal at the combinatorial gate;

receiving a clock signal at the combinatorial gate; and,

providing an output corresponding to the clock signal when the output of the combinatorial gate corresponds to the clock signal; and,

providing an output having a near domino function when the output of the combinatorial gate corresponds to the data signal.

12. The method of claim 11 wherein:

the near domino function is provided based upon performing a reverse traversal function on a circuit design containing the combinatorial gate.

13. The method of claim 11 wherein:

the near domino function includes causing a later arriving edge of the data signal to cause the output signal to respond.

14. The method of claim 11 wherein:

the data signal includes a single edge per clock period; and,

when providing the near domino function, the single edge is propagated through the combinatorial gate.

15. The method of claim 11 wherein:

the clock signal includes two edges per clock period; and,

when providing the clock signal as the output, the two edges are propagated through the combinatorial gate.

16. A static timing engine comprising:
a data model, the data model including a combinational block determinator module, the combinational block determinator module including
means for performing a reverse traversal function on a circuit containing the combinatorial gate, and
a timing engine portion coupled to the data model, the timing engine portion including
means for modeling an output of the combinatorial gate as a clock signal when an input to a next element of the circuit is clock input; and,
means for modeling the output of the combinatorial gate as a data signal when an input to a next element of the circuit is a data input.

17. The static timing engine of claim 16 wherein:
the means for modeling the output of the combinatorial gate as a data signal includes means for modeling a near domino function.

18. The static timing engine of claim 17 wherein:
the near domino function includes causing a later arriving edge of the data signal to cause the output signal to respond.

19. The static timing engine of claim 17 wherein:
the data signal includes a single edge per clock period; and,
when providing the near domino function, the single edge is propagated through the combinatorial gate.

20. The static timing engine of claim 17 wherein:
the clock signal includes two edges per clock period; and,
when propagating the clock signal, the two edges are propagated through the combinatorial gate.